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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,393	12/09/2003	Chaiyuth Chansungsan	884.A83US1	4663

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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,393	CHANSUNGSAN ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 5-20* is/are rejected.

7)☒ Claim(s) *2-4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/24/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 6/24/2005. Claims 1-20 are pending and are under examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 15 and 17-20 remain rejected under 35 U.S.C. 102(b) as being anticipated by Yoshimura (USP 5,629,642). Figure 2 of Yoshimura shows a noise detector circuit for detecting noise in power supply comprising receiving a substantially noise free current signal (constant voltage generator 19 having a noise free 127 shown in figure 8), receiving one or more power supply signals (Vcc and ground), processing the substantially noise free curent signal and the one or two power supply signals to detect noise signal in the one or two power supply signals and generating a noise detection signal (output of the comparator 20) in response to detection of noise signal as called for in claims 15, 18.

Regarding claim 17, figure 2 shows Vcc and ground are two voltage having different polarities (positive and negative).

Regarding claim 19, the output of the comparator 20 is a digital signal in response to the detection of noise signal.

Regarding claim 20, the noise detection threshold level is set by the generator 19 and the calibration potential level, the voltage level slightly above the ambient noise in the system, is embedded within the power supplies.

3. Claims 15 and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Uchimura et al. (USP 4,622,480), prior art of record. Figure 7 of Uchimura et al. shows a noise detector circuit for detecting noise in power supply comprising producing a substantially noise free current signal (the current flows the transistor 90 of figure 8 is noise free signal), detecting one or more power supplies Vdd, processing the substantially noise free curent signal and the one or two power supply signals to detect noise signal in the one or two power supply signals and generating a noise detection signal (output Vbout) in response to detection of noise signal as called for in claims 15 and 18.

Regarding claim 17, figure 2 shows Vdd and ground are two voltage having different polarities (positive and negative).

Regarding claim 19, the output of the comparator 20 is a digital signal in response to the detection of noise signal.

Regarding claim 20, the noise detection threshold level is set by the VBIN as the calibration potential level, the voltage level slightly above the ambient noise in the system, is embedded within the power supplies.

4. Claims 1 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Uchimura et al. (USP 4,622,480), prior art of record. Figure 7 of Uchimura et al. shows a noise detector circuit (73, 61-72) for detecting noise in power supply comprising a reference current source (74 details shown in figure 8) to provide a substantially noise free differential current signal (the

differential current flows through the transistors 90 and 92), a detector (73, 61-72) coupled to one or two power supplies, the detector to receive the substantially noise free differential current signal, to detect a noise signal on the one and/or two power supplies, and to generate a high noise detection signal to indicate detection of the noise signal as called for in claims 1 and 16.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchimura (USP 4,622,480). Figure 7 of Uchimura et al. shows a noise detector circuit (73, 61-72) for detecting noise in power supply comprising a reference current source (74 details shown in figure 8) to provide a substantially noise free differential current signal (the differential current flows through the transistors 90 and 92), a detector (73, 61-72) coupled to one or two power supplies, the detector to receive the substantially noise free differential current signal, to detect a noise signal on the one and/or two power supplies, and to generate a high noise detection signal to indicate detection of the noise signal.

The differences seen between Uchimura et al. reference and the present invention is that the Uchimura et al. shows a single reference current source and a single power supplies detector instead of a plurality of reference current sources and a corresponding plurality of power supplies detector as called for in claims 5-14. However, one skilled in the art would have been recognized that Uchimura et al. power supplies detection circuit can be expanded by duplicating

a plurality of each reference current circuits and power supplies detector circuits. Such expansion is seen as an obvious modification to one skilled in the art for sensing plurality of power supplies. Therefore, outside of non-obvious results, the obviousness of duplicating a plurality of each reference current circuits and power supplies detector circuits will be patentable under 35USC 103(a).

Regarding claims 6-14, the limitations recited therein are seen to be inherently present in Uchimura et al.

Response to Arguments

7. Applicant's arguments filed 6/24/2005 have been fully considered but they are not persuasive. Applicant argues that Yoshimura produces a constant voltage not a substantially noise free current signal as called for in claim 15 is not persuasive. By Ohm's law V=IR there is constant associated with a constant voltage generated by the voltage generator 19 of Yoshimura. Since the current is constant thus it is noise free signal. Therefore, the limitation of noise free current is also met. Therefore, the limitations of claims 15 and 17-20 are deemed to be proper.

Allowable Subject Matter

8. Claims 2-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

7/26/2005